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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,178	02/13/2004	Jian-Shen Yu	10929-US-PA	2177

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
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ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER

NGUYEN, JIMMY H

ART UNIT PAPER NUMBER

2629

DATE MAILED: 11/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/708,178

Applicant(s)

YU ET AL.

Examiner

Jimmy H. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☒ Claim(s) 9-12 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is made in response to applicant's papers filed on 02/13/2004. Claims 1-12 are currently pending in the application. An action follows below:

Notice to Applicants

2. It is not appropriate to use the term, "a control signal **module**" to define a signal. See Fig. 5A; specification, paragraph 0032; and claim 8. It is in the best interest of the patent community that applicant, in his/her normal review and/or rewriting of the specification, drawing, and claims, to take into consideration these editorial situations and make changes as necessary.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features, "the output buffer comprises an odd number of **inverters**" of claim 4, "the output buffer is made of complementary metal-oxide-semiconductor (CMOS) **inverter**" of claim 5, "the level shifter comprises a plurality of **inverters** that are made of n-type thin film transistor and p-type thin film transistor" of claim 6, and "the **inverters** of the level shifter have a thin film transistor that is self-connected drain/source and gate" of claim 7, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure

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must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claim 3 is objected to under 37 CFR 1.75(a) because although this claim meets the requirement 112/2d, i.e., the metes and bounds are determinable, however, the following changes should be made:

- a. delete "one of" in line 5 because a clock signal must have two levels; and
- b. insert -- to a target signal -- immediately after "the relay signal" in line 14 (see claim 1, line 16).

Appropriate correction is required.

5. Claim 8 is objected to under 37 CFR 1.75(a) because although this claim meets the requirement 112/2d, i.e., the metes and bounds are determinable, however, "the dynamic register couples the clock input terminal to the level shifter, and determines whether to conduct the clock input terminal to the level shifter according to a control signal module." should be changed to -- the dynamic register couples to the clock input terminal, for receiving the clock signal, and determines whether to provide the clock signal to the level shifter, in according to a control

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signal.”, so as to make the claimed invention consistent with the specification, see paragraph 0032.

6. Claim 9 is objected to because of the following informalities:

- a. change “stage, and determines” in lines 5-6 to -- stage and determining --;
- b. change “input terminal” in line 6 to -- signal --; and
- c. change “stage, and determines” in lines 10-11 to -- stage and determining --.

Appropriate correction is required.

7. Claim 10 is objected to because of the following informalities:

- a. insert -- register -- immediately after “dynamic” in line 2;
- b. change “stage, and determines” in lines 5-6 to -- stage and determining --;
- c. change “input terminal” in line 6 to -- signal --; and
- d. change “shifter, and determines” in lines 10-11 to -- shifter and determining --.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 4-7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

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As per claims above, these claims contain the features, “the output buffer comprises an odd number of **inverters**” of claim 4, “the output buffer is made of complementary metal-oxide-semiconductor (CMOS) **inverter**” of claim 5, “the level shifter comprises a plurality of **inverters** that are made of n-type thin film transistor and p-type thin film transistor” of claim 6, and “the **inverters** of the level shifter have a thin film transistor that is self-connected drain/source and gate” of claim 7, which were not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Since the specification does not describe expressly the above underlined features at all, a person of ordinary skill in the art at the time of the invention was made can't recognize how many inverters are included, how the inverters are connected, and what the inverters function, in the output buffer or in the level shifter. Accordingly, these claims contain the above underlined features, which were not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claim 7, this claim recites a feature, “a thin film transistor that is self-connected drain/source and gate”. Since it is unclear what the applicant means “drain/source”, i.e., “drain or source” or “drain and source”, it is considered that the invention is not clearly defined.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 1-3 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicants'

Admitted Prior Art, hereinafter AAPA.

As to claim 1, As noting in Figs. 2A and 2B and the specification, paragraph 0009, AAPA discloses an amplifying method of a clock signal (CLK in) of an liquid crystal display (LCD) driving circuit (see paragraph 0009), for amplifying a periodic clock signal (CLK in) swinging between a first original level (3V) (see Fig. 2B) and a second original level (GND or 0V) to a target signal (an output signal of the second level shifter 209, see Fig. 2B) swinging between a first target level (a positive voltage VDD) and a second target level (a negative voltage VSS), wherein the first original level (3V) is higher than the second original level (GND or 0V), the first target level (VDD) is higher than the second target level (VSS), the first target level (VDD) is higher than the first original level (3V), and the second target level (VSS) is lower than the second original level (GND or 0V), the amplifying method for a clock signal of an LCD driving circuit comprising: amplifying the clock signal (CLK in) to a relay signal (an output signal of the first level shifter 203, see Fig. 2B) that swings between a first relay level (a positive voltage VDD) and a second relay level (GND), wherein the first relay level (VDD) is higher than the second relay level (GND); and amplifying the relay signal to the target signal,

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wherein the first relay level (VDD) is the first target level (VDD) (i.e., between the first original level (3V) and the first target level (VDD)) and the second relay level (GND) is the second original level (GND) (i.e., between the second original level (GND) and the second target level (VSS)). Accordingly, the claimed limitations are read in AAPA.

As to claim 2, as noting in Fig. 2A, AAPA discloses the first level shifter (203) receiving the clock signal during a period, which inherently begins when a user turns a display on and ends when a user turns the display off (i.e., a predetermined period).

As to claim 3, as noting in Fig. 1 and paragraph 0008 of the specification, AAPA discloses a driving stage for an LCD driving circuit (see paragraph 0008), the driving stage being part of the LCD driving circuit in a cascade fashion, the driving stage comprising: a clock input terminal (CLK in terminal, see Fig. 1), for receiving a clock signal (CLK) having a first original level (3V) and a second original level (GND or 0V); a level shifter (a circuit including elements 105 and 110, see Fig. 1), coupling to the clock input terminal (CLK in), for receiving the clock signal (CLK) from the clock input terminal, operating at a first target level (a positive voltage VDD) and a second target level (a negative voltage VSS), for amplifying the clock signal to a relay signal (an output of the element 110, see Fig. 1) having a first relay level (VDD) and a second relay level (VSS); and an output buffer (115), coupling to the level shifter (110), for receiving the relay signal from the level shifter, operating at the first target level (VDD) and the second target level (VSS), for amplifying the relay signal having one of the first target level and the second target level, wherein the first original level (3V) is higher than the second original level (GND), the first target level (VDD) is higher than the second target level (VSS), the first relay level (VDD) is the first target level (i.e., between the first original level (3V) and the first

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target level (VDD)), and the second relay level (VSS) is the second target level (i.e., between the second original level (GND) and the second target level (VSS)). Accordingly, the claimed limitations are read in AAPA.

14. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki et al. (US 6,392,628 B1), hereinafter Yamazaki.

As to claim 1, As noting in Fig. 9, Yamazaki discloses an amplifying method of a clock signal (CLK) of an liquid crystal display (LCD) driving circuit (see paragraph 0009), for amplifying a periodic clock signal (CLK in) swinging between a first original level (3V) (see Fig. 9) and a second original level (GND or 0V) to a target signal (an output signal of the second level shifter circuit (see Fig. 9) swinging between a first target level (+10V, see Fig. 9, col. 22, lines 59-67, col. 1, line 63 through col. 2, line 3, and col. 3, lines 19-37) and a second target level (-10V, see Fig. 9, col. 22, lines 59-67, col. 1, line 63 through col. 2, line 3, and col. 3, lines 19-37), wherein the first original level (3V) is higher than the second original level (GND or 0V), the first target level (+10V) is higher than the second target level (-10V), the first target level (+10V) is higher than the first original level (3V), and the second target level (-10V) is lower than the second original level (GND or 0V), the amplifying method for a clock signal of an LCD driving circuit comprising: amplifying the clock signal (CLK) to a relay signal (an output signal of the shifter register circuit, see Fig. 9) that swings between a first relay level (+5V, see Fig. 9, col. 22, lines 35-38, col. 1, line 63 through col. 2, line 3, and col. 3, lines 19-37) and a second relay level (-5V) (see Fig. 9, col. 22, lines 35-38, col. 1, line 63 through col. 2, line 3, and col. 3, lines 19-37), by using the first level shifter circuit and the shift register circuit, wherein the first relay level (+5V) is higher than the second relay level (-5V); and amplifying the relay signal to

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the target signal, wherein the first relay level (+5V) is between the first original level (3V) and the first target level (+10V) and the second relay level (-5V) is between the second original level (GND) and the second target level (-10V). Accordingly, the claimed limitations are read in the Yamazaki reference.

As to claim 2, as noting in Fig. 9, Yamazaki discloses the first level shifter circuit receiving the clock signal (CLK) during a period, which inherently begins when a user turns a display on and ends when a user turns the display off (i.e., a predetermined period).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

16. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, as applied to claim 3 above, and further in view of Maekawa et al. (US: 5,646,642), hereinafter Maekawa.

As to claim 8, as discussed in the rejection to claim 3 above, AAPA discloses all the claimed limitations except for a dynamic register, as defined in claim 8. However, Schmidt discloses a related driving stage comprising a dynamic register (a detecting/offsetting circuit 1A, see Fig. 1) receiving a clock signal (CK1) and determining whether to provide the clock signal to the level shifter (a level shifting circuit 2, see Fig. 1, col. 4, line 56) according to a control signal (a signal is supplied to the gate electrode of TFT mpA, see Fig. 1), see col. 4, lines 50 through col. 5, line 27). It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide the dynamic register in the driving stage of AAPA, in view of

the teaching in the Maekawa reference, because this would provide a level converting circuit which operate stably for any clock signal having a low amplitude, as taught by Maekawa.

Allowable Subject Matter

17. Claims 9-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and if overcome the claim objections above.

18. The following is a statement of reasons for the indication of allowable subject matter: the claimed invention is directed to a driving stage for an LCD driving circuit in a cascade fashion. Dependent claim 9 identifies the uniquely distinct feature, "the dynamic register comprises ... to the next stage driving signal", as presently recited in lines 1-13. Dependent claim 10 identifies the uniquely distinct feature, "the dynamic register comprises ... thereby", as presently recited in lines 1-12. The closest prior arts, AAPA and Yamazaki discussed in the rejections above, either singularly or in combination, fail to anticipate or render the above underlined limitations obvious.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kubota et al. (US 6,300,927 B1) discloses a related driving stage for an LCD driving circuit and an amplifying method of a clock signal, see Figs. 7 and 8 and Abstract.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy H. Nguyen whose telephone number is 571-272-7675.


The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m..

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached at 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JHN
November 16, 2006



Jimmy H. Nguyen
Primary Examiner
Technology Division: 2629